IN THE SPECIFICATION

Please amend the paragraph beginning at page 49, line 23, as follows:

FIG. 11 shows a sectional view of the active matrix liquid crystal display device taken along the line 11-11 of FIG. 10. Reference numeral 401 denotes a glass substrate, 402 a gate electrode, 403 a gate insulating film, ~~404 an island-shaped protrusion layer on which island-shaped protrusions with a low surface energy are scattered~~, 405 a source electrode, 406 a drain electrode, 407 a pentacene vapor-deposited film, 408 and 408' signal wires, 409 and 409' scanning wires, 410 a pixel electrode, 411 a SiNx protective film, 413 and 413' oriented films, 414 ~~an opposed electrode~~ a glass substrate, 415 ~~a liquid crystal composition~~ an opposed electrode, 416 ~~a gap~~ a liquid crystal composition, 417 a spacer bead, 418 and 418' polarization plates, 419 a TFT substrate, and 420 an opposed substrate. Reference numeral 404 denotes an interface between the pentacene vapor-deposited film 407 and the gate insulating film 403. FIGS. 12A through 12C show the production steps (Steps 601 through 622) for the active matrix substrate display device shown in FIGS. 10 and 11.

Please amend the paragraph beginning at page 53, line 16, as follows:

As for the explanation of FIG. 13, FIG. 13 shows a portion of an IC substrate. For simplicity of FIG. 13, only one inverted TFT is shown, but this one device is a large integrated array device. In Fig. 13, reference character 508 denotes a silicon substrate, 509 an organic semiconductor layer, 510 a resin insulating film, 512 a lower electrode, 514 a ferroelectric layer, 516 an upper electrode, 518 a resin insulating film, 528

an insulating film, 529 a metal wiring, 526 a conductive layer formed by embedding a metal in a through-hole, S a source electrode, and D a drain electrode. Additionally, the elements and the like shown in the figure are not accurately scaled. The IC information tag in the present Example has a structure in which an organic semiconductor is arranged on the downside, and a dielectric memory is stacked thereover. In the present invention, an organic dielectric memory is used, and two transistors are used to operate the memory. If the degree of integration is not taken into account, an inorganic dielectric can be combined in one and the same plane. A structure is also possible in which one dielectric is allotted to one transistor. Additionally, an organic transistor may be formed on an organic dielectric memory, in a reversed manner.